CHAPTER 4

Operational Amplifier Basics

Syllabus

- Basic physics of MOS transistors and their equivalent circuit models (ch. 6)
- Elementary gain stages (ch. 7, ch. 9, and ch. 10)
- Operational amplifier basics (ch. 8)
- Frequency responses (ch. 11)
- Noise (ch.7, Design of analog CMOS ICs)
- Feedback, stability and compensation (ch. 12)
- Operational amplifiers (ch.9, Design of analog CMOS ICs)

Operational Amplifiers

- 1940, well before the invention of the transistor
- Realized by vacuum tubes
  - Electronic integrators, differentiators, etc.
  - “Analog computers”
- Each op amp implemented a math *operation*

General Concepts

- Op Amp Properties

Linear Op Amp Circuits

- Noninverting Amplfier
- Inverting Amplifier
- Inetgrator and Differentiator
- Voltage Added

Nonlinear Op Amp Circuits

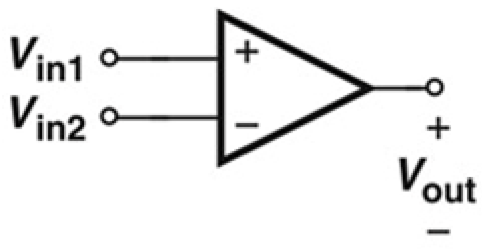
- Precision Rectifier
- Logarithmic Amplifier
- Square Root Circuit

Op Amp Nonidealities

- DC Offsets
- Input Bias Currents
- Speed Limitations
- Finite Input and Output Impedances

Basic Operational Amplifier

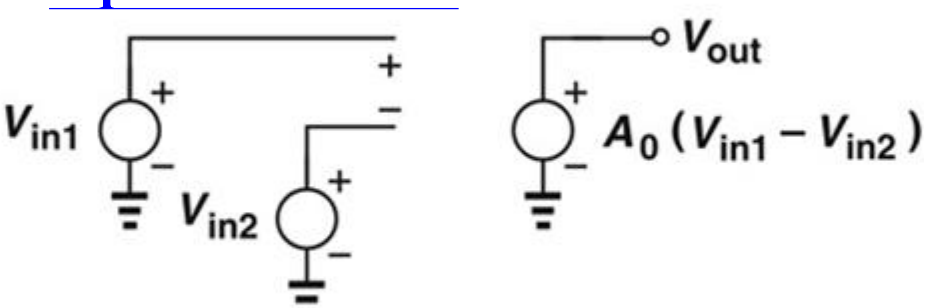
Op amp as a black box



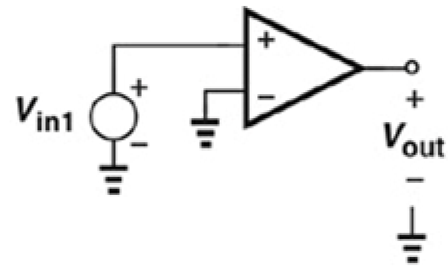
$$V_{out} = A_0(V_{in1} - V_{in2}).$$

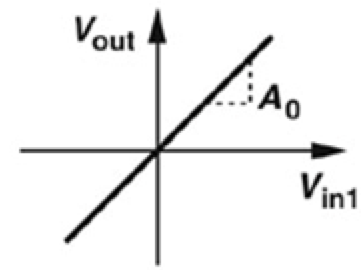
V_{in1}: non-inverting input
V_{in2}: inverting input
A_0: open-loop gain

Equivalent circuit

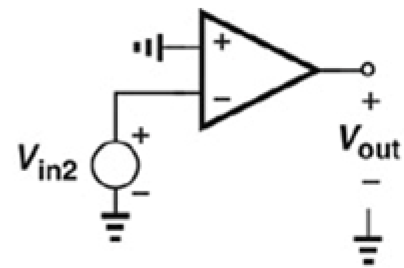


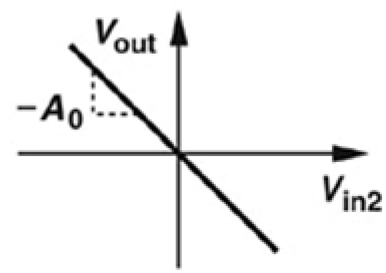
$V_{in2}=0$, $V_{out} = A_0V_{in1}$





$V_{in1}=0$, $V_{out} = -A_0V_{in2}$

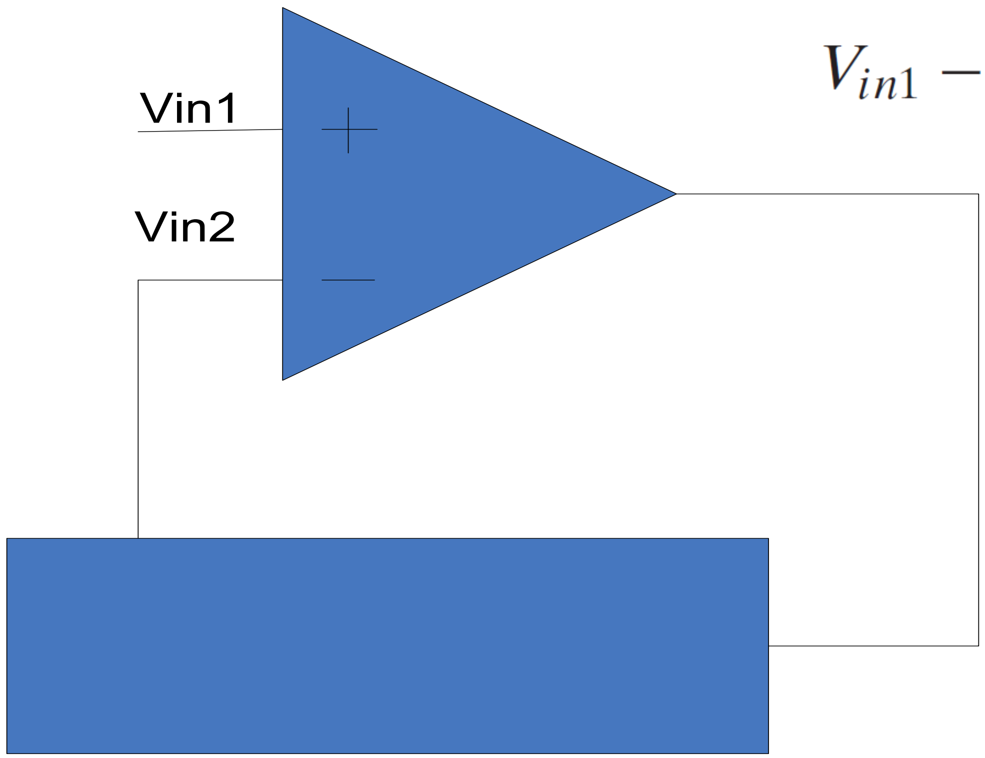




An ideal op amp

1. **Infinite voltage gain**
2. **Infinite input impedance**
3. **Zero output impedance**
4. **Infinite speed**

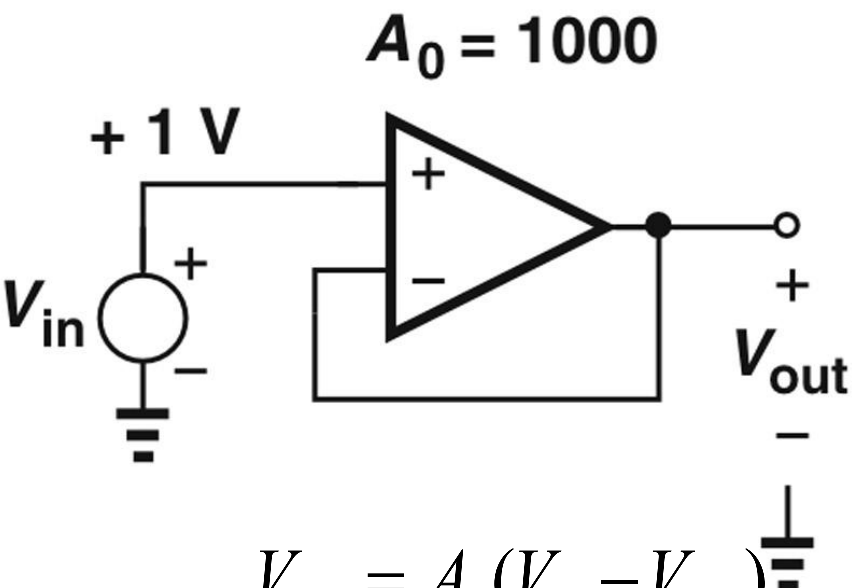
Virtual Short of the Op Amp



$$V_{in1} - V_{in2} = \frac{V_{out}}{A_0}$$

- **Due to infinite gain of op amp, the circuit forces V_{in2} to be close to V_{in1}, thus creating a virtual short.**
- **Virtual short is *NOT* a short!!**

Unity-Gain Amplifier (Buffer)

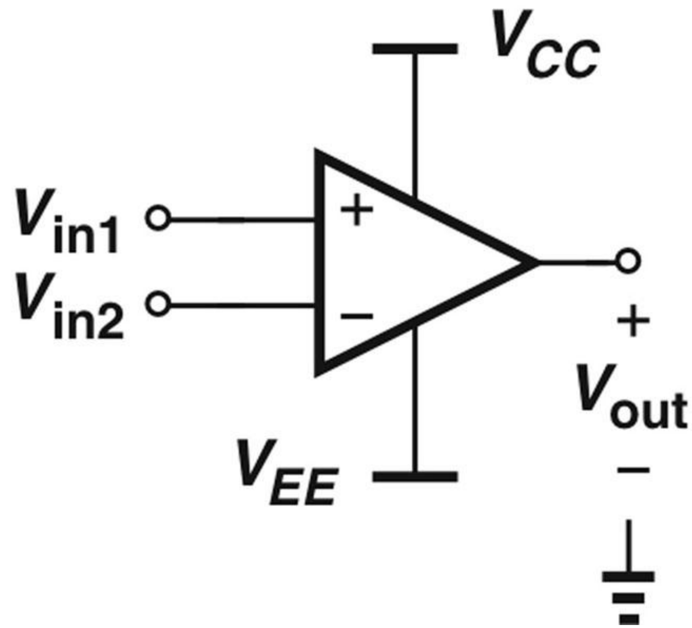


$$V_{out} = A_0(V_{in} - V_{out})$$

$$\frac{V_{out}}{V_{in}} = \frac{A_0}{1 + A_0}$$

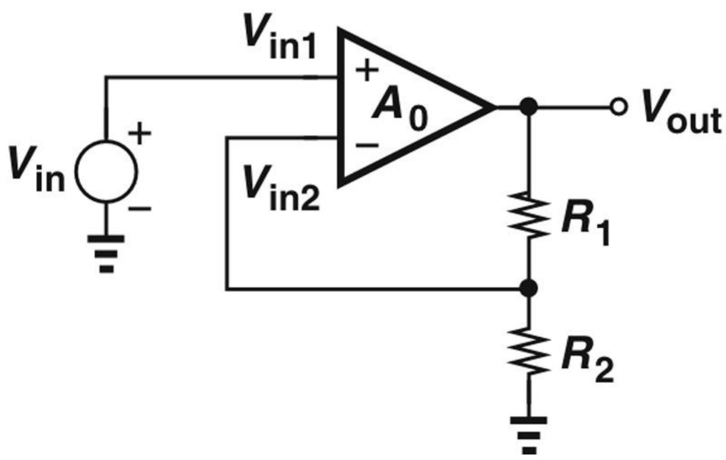
$A_0 = 1000$, $V_{in} = 1V$, $V_{out} = 0.999V$

Op amp with power supplies



- **Remember: The op amp needs supply voltages V_{CC} and V_{EE} to function.**

Noninverting Amplifier



$$V_{in2} = \frac{R_2}{R_1 + R_2} V_{out}$$

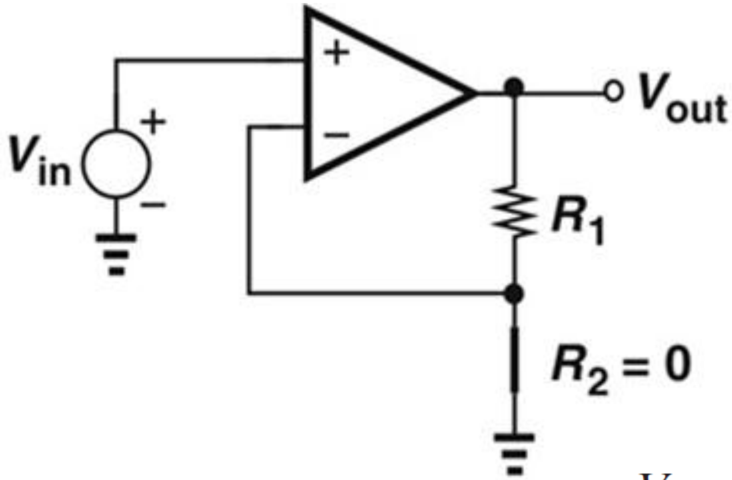
$$\Rightarrow \quad V_{in1} \approx V_{in2} \approx \frac{R_2}{R_1 + R_2} V_{out}$$

$$\Rightarrow \quad \frac{V_{out}}{V_{in}} \approx 1 + \frac{R_1}{R_2}$$

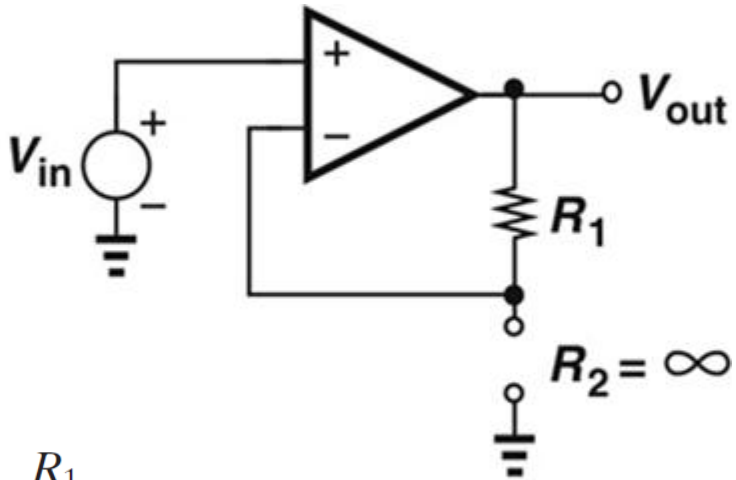
- **Positive gain: the circuit is called a "noninverting amplifier".**
- **The result is the "closed-loop" gain of the circuit.**
- **The voltage gain depends on only the *ratio* of the resistors.**
  - **The idea of creating dependence on only the ratio of quantities that have the same dimension plays a central role in circuit design.**

Two Extreme Cases

(1) $R_1/R_2 \rightarrow \infty$



(2) $R_1/R_2 \rightarrow 0$



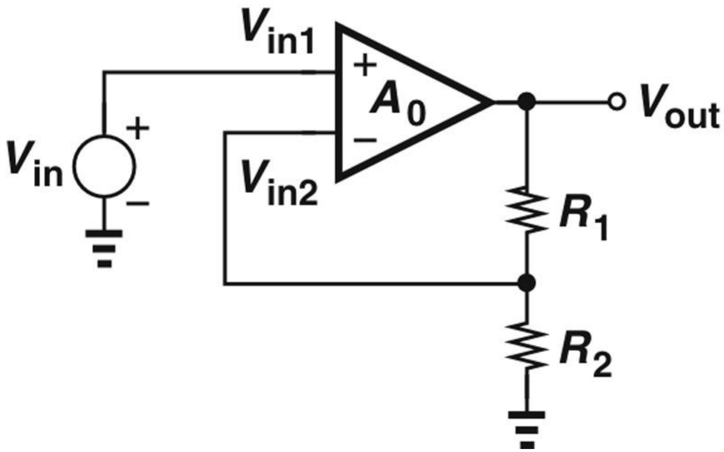
$$\frac{V_{out}}{V_{in}} \approx 1 + \frac{R_1}{R_2}$$

$V_{out}/V_{in} \rightarrow \infty$

$V_{out}/V_{in} \rightarrow 1$

- **With the ratio between R_1/R_2 varies, the noninverting amplifier configuration behaves from open-loop op amp to unity-gain buffer.**

Noninverting Amp with Finite Gain



$$(V_{in1} - V_{in2})A_0 = V_{out}$$

$$V_{in2} = \frac{R_2}{R_1 + R_2} V_{out}$$

$$\frac{V_{out}}{V_{in}} = \frac{A_0}{1 + \frac{R_2}{R_1 + R_2} A_0} \approx 1 + \frac{R_1}{R_2}$$

$$A_0 R_2/(R_1 + R_2) \gg 1$$

Two gains

1. **"Open-loop" gain: The gain of the op amp: A_0**
2. **"Closed-loop" gain: The gain of the overall amplifier: $1+R_1/R_2$**

Gain error

The finite gain of the op amp creates A small error

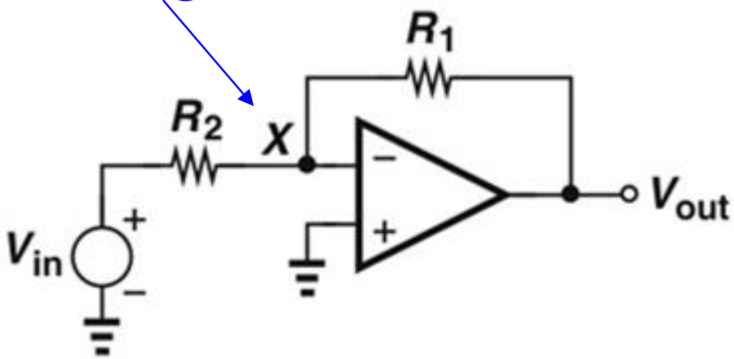
$$(1+\epsilon)^{-1} \approx 1 - \epsilon \text{ for } \epsilon \ll 1$$

$$\frac{V_{out}}{V_{in}} \approx \left(1 + \frac{R_1}{R_2}\right)\left[1 - \underbrace{\left(1 + \frac{R_1}{R_2}\right)\frac{1}{A_0}}_{\text{Gain error}}\right]$$

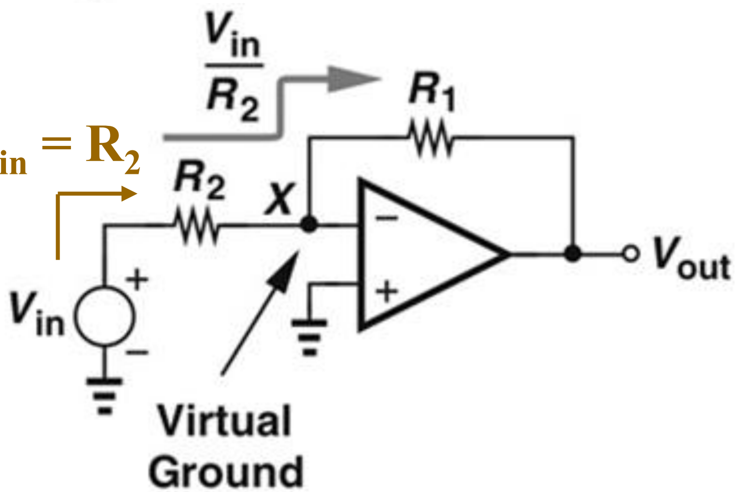
- **A higher closed-loop gain is accompanied with a greater gain error.**

Inverting Amplifier

Virtual ground

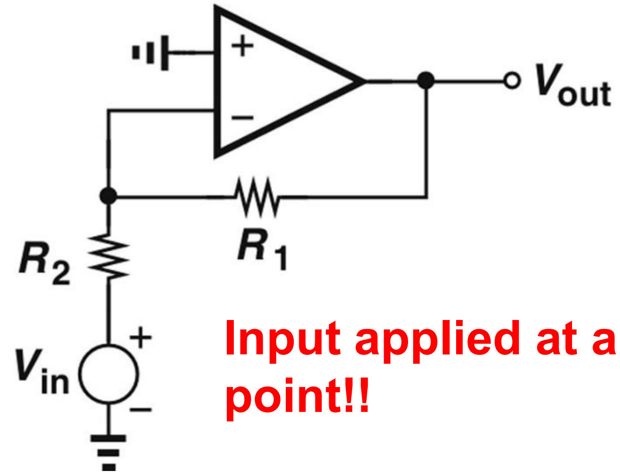


$R_{in} = R_2$



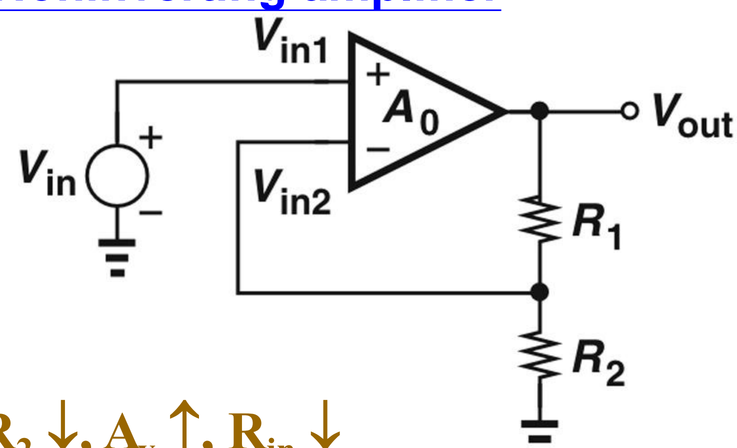
$$\frac{0 - V_{out}}{R_1} = \frac{V_{in}}{R_2} \Rightarrow \frac{V_{out}}{V_{in}} = \frac{-R_1}{R_2}$$

Another look



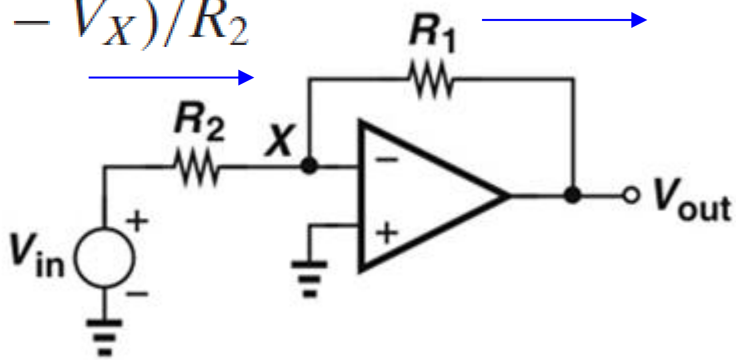
Input applied at a different point!!

Noninverting amplifier



$R_2 \downarrow, A_v \uparrow, R_{in} \downarrow$

Inverting Amp with Finite Gain



$$V_{out} = A_0(V_{in1} - V_{in2}) = -A_0 V_X$$

$$\Rightarrow \frac{V_{out}}{V_{in}} = -\frac{1}{\frac{1}{A_0} + \frac{R_2}{R_1}\left(\frac{1}{A_0} + 1\right)}$$

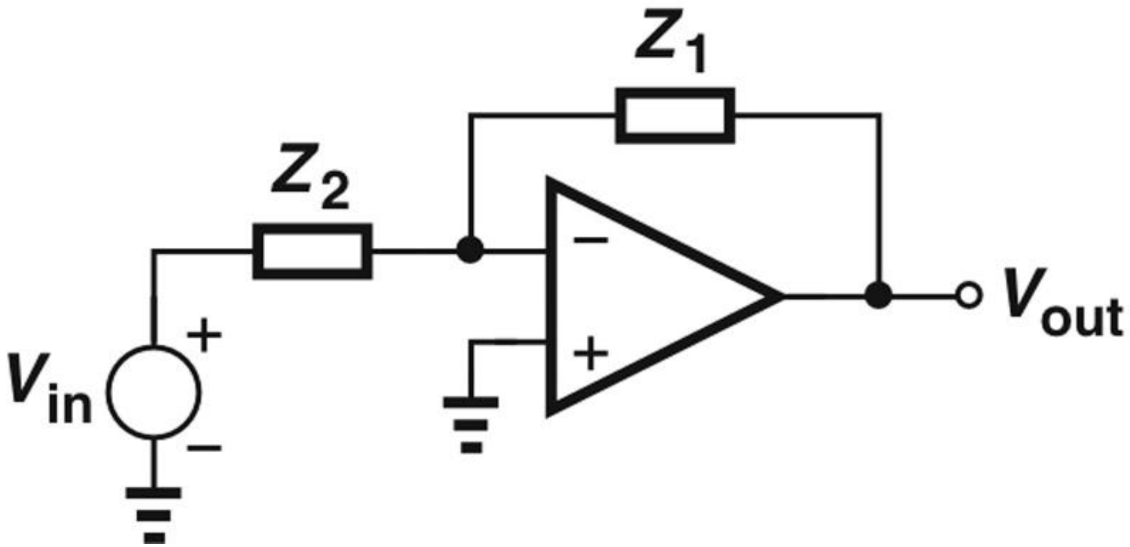
$$= -\frac{1}{\frac{R_2}{R_1} + \frac{1}{A_0}\left(1 + \frac{R_2}{R_1}\right)}$$

assuming $(1 + R_1/R_2)/A_0 \ll 1$

$$\frac{V_{out}}{V_{in}} \approx -\frac{R_1}{R_2}\Big[1 - \underbrace{\frac{1}{A_0}\Big(1 + \frac{R_1}{R_2}\Big)}_{\text{Gain error}}\Big]$$

- **A higher closed-loop gain is accompanied with a greater gain error.**
- **The gain error expression is the same for noninverting and inverting amplifiers.**

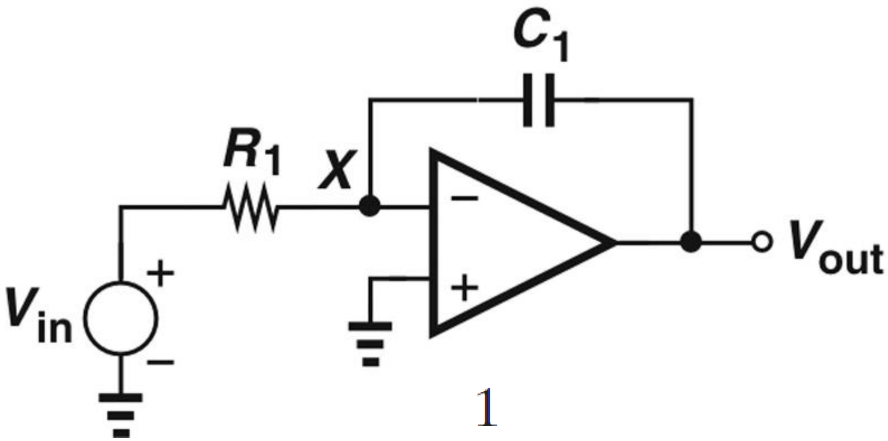
Circuit with General Impedances



$$\frac{V_{out}}{V_{in}} \approx -\frac{Z_1}{Z_2}$$

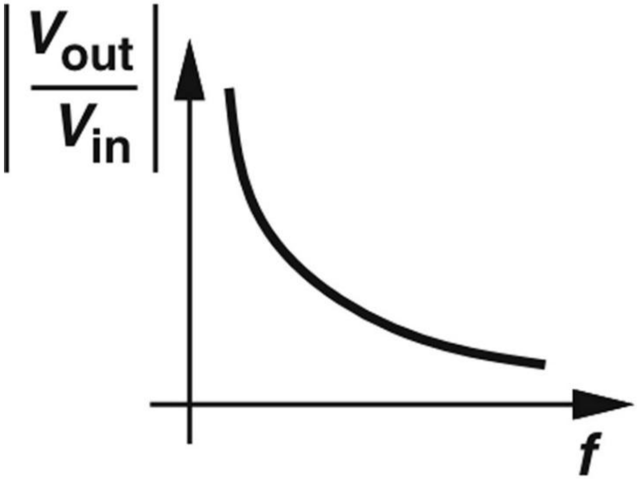
- It is possible to employ complex impedances instead of resistors.
- If Z_1 or Z_2 is a capacitor, two interesting functions result.

Integrator



$$\frac{V_{out}}{V_{in}} = -\frac{\frac{1}{C_1 s}}{R_1} = -\frac{1}{R_1 C_1 s}$$

Frequency response



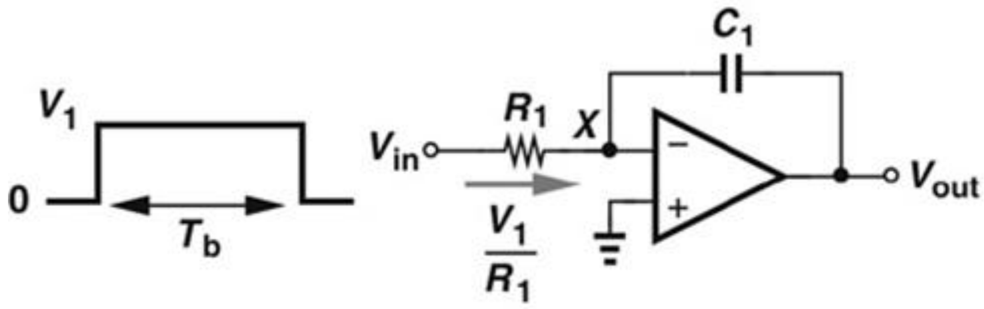
Time domain

$$\frac{V_{in}}{R_1} = -C_1 \frac{dV_{out}}{dt} \Rightarrow V_{out} = -\frac{1}{R_1 C_1} \int V_{in}\, dt$$

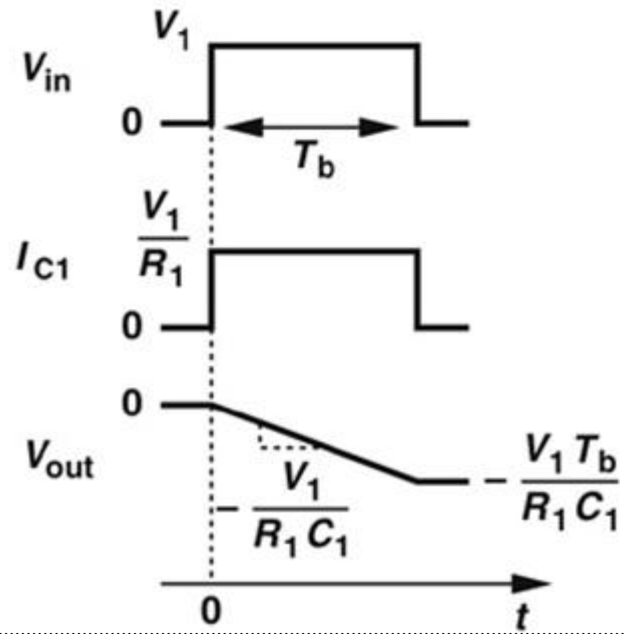
➢ **If Z_1 is a capacitor and Z_2 is a resistor, an integrator is achieved.**

Integrator with Pulse Input

Assume a zero initial condition across C_1 and an ideal op amp



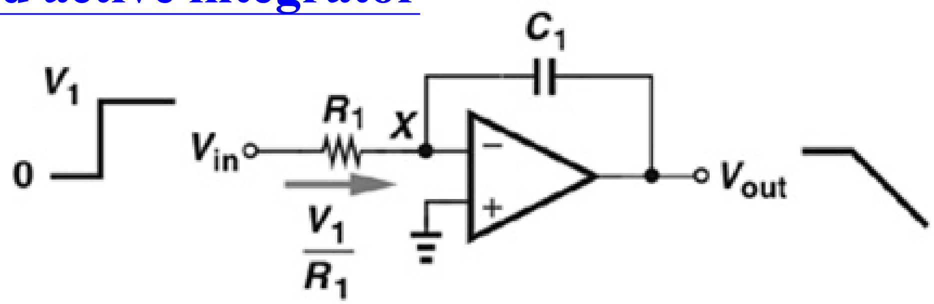
$$V_{out} = -\frac{1}{R_1 C_1}\int V_{in}\,dt = -\frac{V_1}{R_1 C_1}t$$



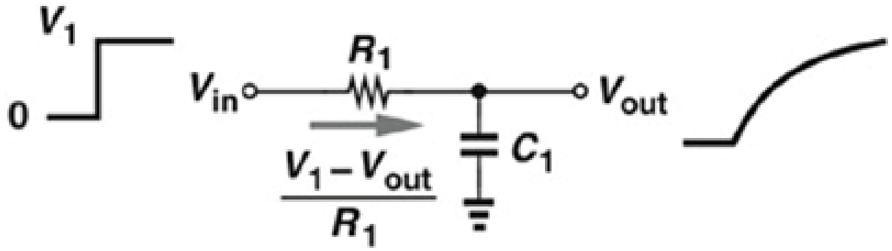
- **The left plate of C_1 is pinned at zero, so only the right plate of C_1 will change.**
- **The output waveform becomes "sharper" as R_1C_1 decreases.**
- **The voltage across the capacitor after the pulse is proportional to the area under the input pulse.**

Comparison of Integrators

Op amp based active integrator

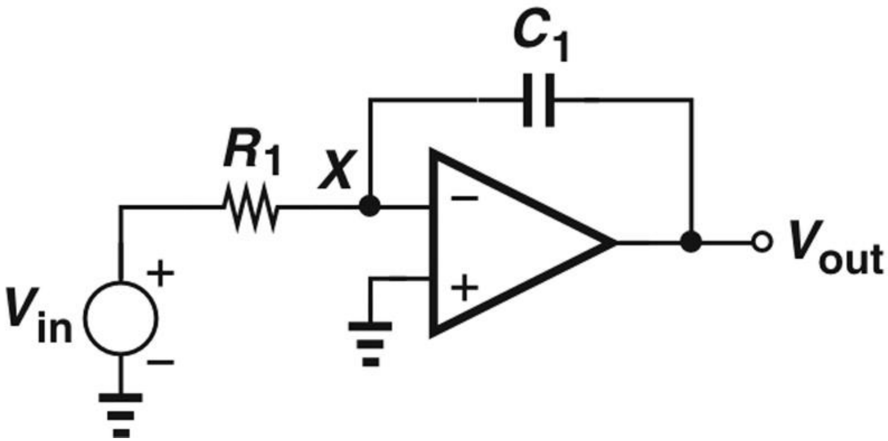


RC low-pass integrator



- The RC low-pass filter is actually a "passive" approximation to an integrator.
- With the RC time constant large enough, the RC filter output approaches a ramp.

Integrator with Finite Gain



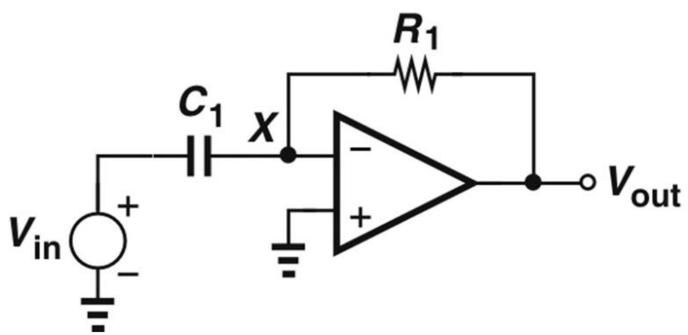
$$\frac{V_{in}-V_X}{R_1}=\frac{V_X-V_{out}}{\frac{1}{C_1 s}} \qquad V_X=\frac{V_{out}}{-A_0}$$

$$\Rightarrow \frac{V_{out}}{V_{in}}=\frac{-1}{\frac{1}{A_0}+\left(1+\frac{1}{A_0}\right)R_1C_1 s}$$

$$s_p=\frac{-1}{(A_0+1)R_1C_1}$$

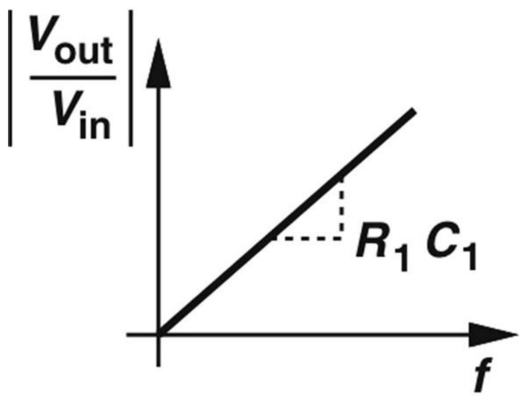
- **When finite op amp gain is considered, the integrator becomes "lossy" as the gain at s = 0 is limited to A_0 (rather than infinity) and the pole moves from the origin to $-1/[(1+A_0)R_1C_1]$.**

Differentiator



$$\frac{V_{out}}{V_{in}} = -\frac{R_1}{\frac{1}{C_1 s}} = -R_1 C_1 s$$

Frequency response



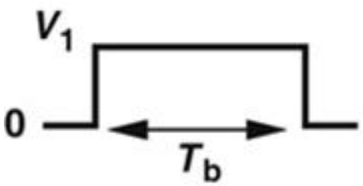
Time domain

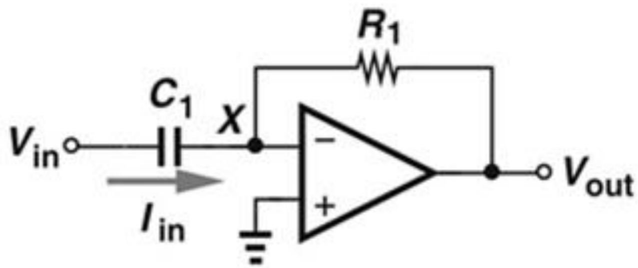
$$C_1 \frac{dV_{in}}{dt} = -\frac{V_{out}}{R_1} \Rightarrow V_{out} = -R_1 C_1 \frac{dV_{in}}{dt}$$

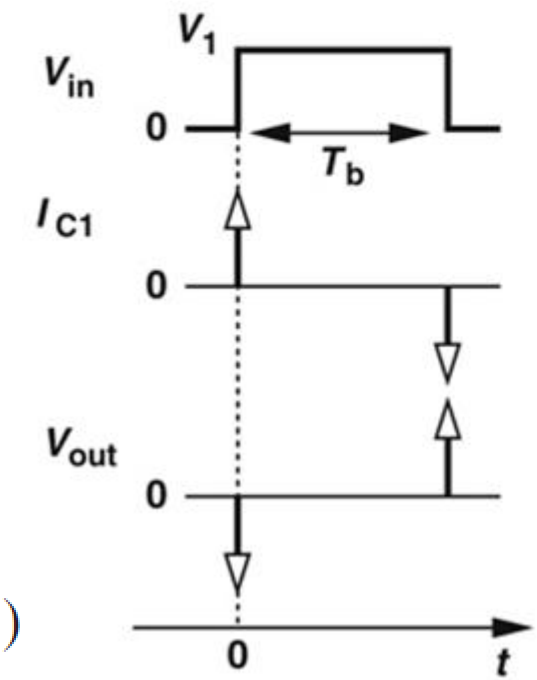
- **If Z_1 is a resistor and Z_2 is a capacitor, an differentiator is achieved.**

Differentiator with Pulse Input

Assume an ideal op amp







At $t = 0^-$, $V_{in} = 0$, $V_{out} = 0$

$$I_{in} = C_1 \frac{dV_{in}}{dt} = C_1 V_1 \delta(t)$$

$$V_{out} = -I_{in} R_1 = -R_1 C_1 V_1 \delta(t)$$

At $t = T_b$, V_{in} returns to 0

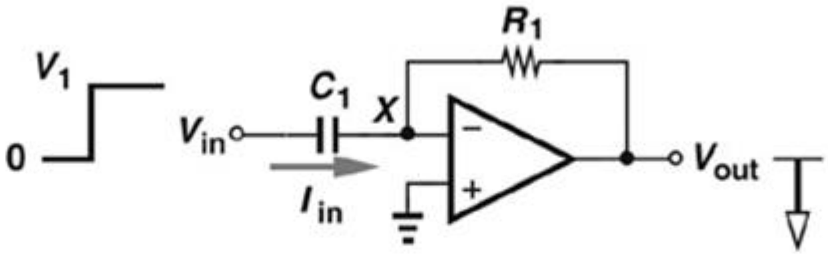
$$I_{in} = C_1 \frac{dV_{in}}{dt} = -C_1 V_1 \delta(t)$$

$$V_{out} = -I_{in} R_1 = R_1 C_1 V_1 \delta(t)$$

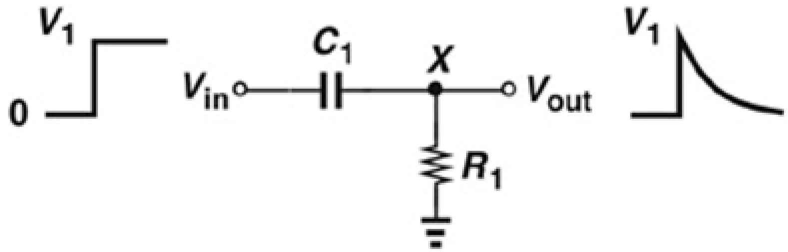
- **The differentiator generates an impulse of current $\pm C_1 V_1 \delta(t)$ and "amplifies" it by R_1 to produce V_{out}.**
- **In reality, the output exhibits neither an infinite height (limited by the supply voltage) nor a zero width (limited by the op amp nonlinearities).**

Comparison of Differentiators

Op amp based active differentiator

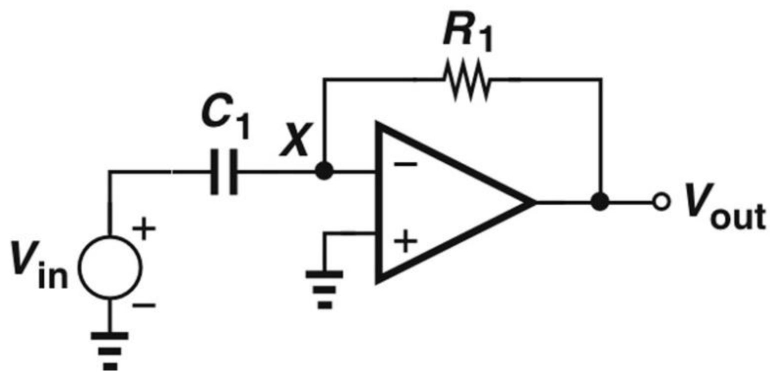


RC low-pass differentiator



- **The RC high-pass filter is actually a "passive" approximation to the differentiator.**
- **With the RC time constant small enough, the RC filter output approximates a differentiator.**

Differentiator with Finite Gain



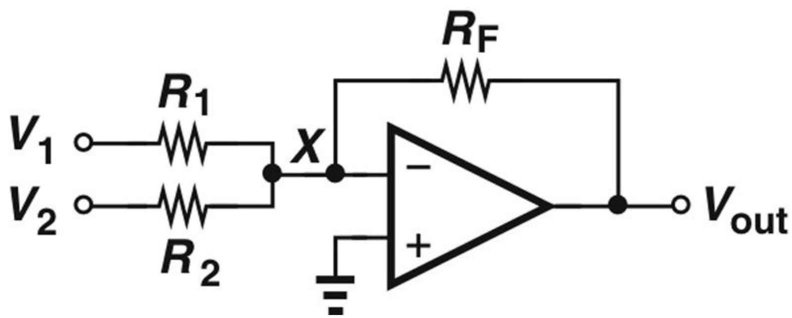
$$\frac{V_{out}}{V_{in}} = \frac{-R_1C_1s}{1+\frac{1}{A_0}+\frac{R_1C_1s}{A_0}}$$

$$\frac{V_{in}-V_X}{\frac{1}{C_1s}} = \frac{V_X - V_{out}}{R_1} \qquad V_X = \frac{V_{out}}{-A_0}$$

$$s_p = -\frac{A_0+1}{R_1C_1}$$

- **When finite op amp gain is considered, the differentiator becomes "lossy" as containing a pole of $-(A_0+1)/R_1C_1$.**
- **It can be approximated as an RC circuit with R reduced by a factor of (A_0+1)**

Voltage Adder



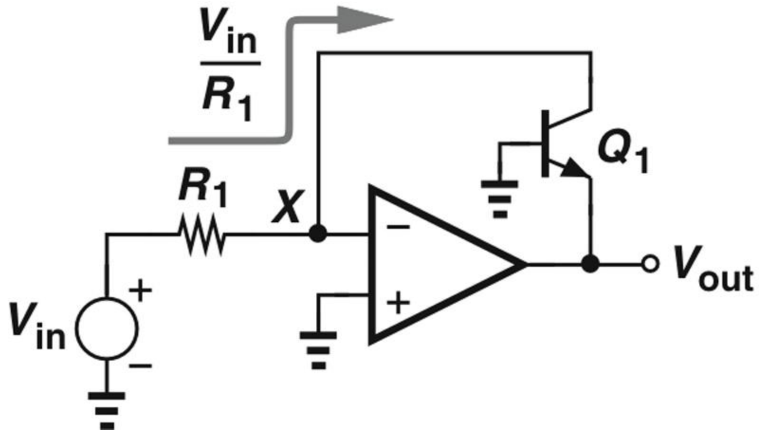
$$\frac{V_1}{R_1} + \frac{V_2}{R_2} = \frac{-V_{out}}{R_F} \quad \Rightarrow \quad V_{out} = -R_F\left(\frac{V_1}{R_1} + \frac{V_2}{R_2}\right)$$

$$R_1 = R_2 = R \quad \Rightarrow \quad V_{out} = \frac{-R_F}{R}(V_1 + V_2)$$

- **Extension to more than two voltages is straightforward.**
- **V_1 and V_2 can be added with different weightings.**

Nonlinear Functions

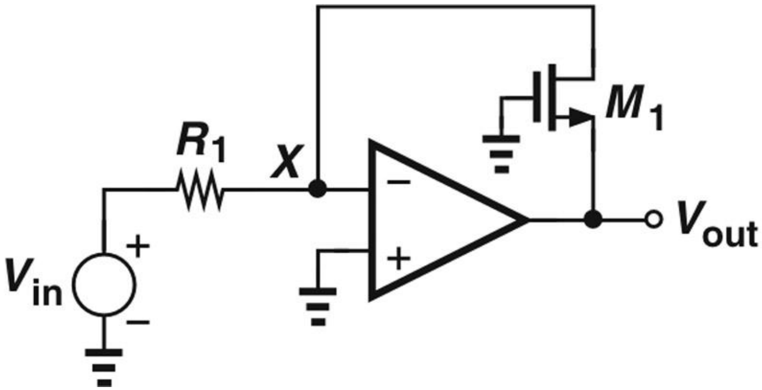
Logarithmic Amplifier



$$V_{BE} = V_T \ln \frac{V_{in}/R_1}{I_S}$$

$$\Rightarrow V_{out} = -V_T \ln \frac{V_{in}}{R_1 I_S}$$

Square-Root Amplifier

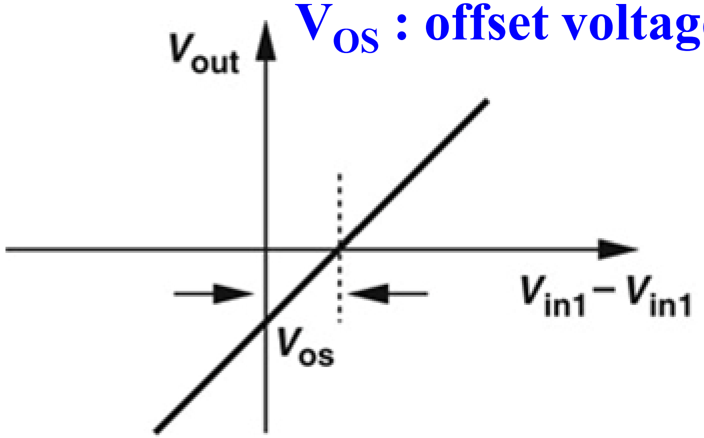


$$\frac{V_{in}}{R_1} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

$$\Rightarrow V_{out} = -\sqrt{\frac{2V_{in}}{\mu_n C_{ox}\frac{W}{L}R_1}} - V_{TH}$$

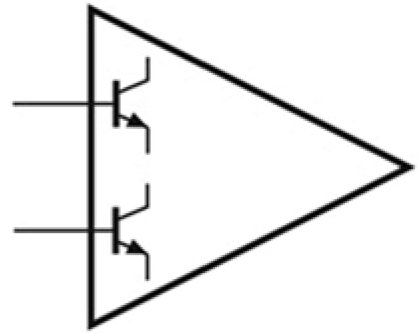
DC Offsets

V_{OS} : offset voltage

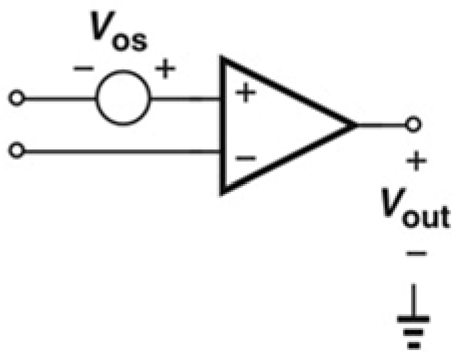


$V_{out} \neq 0$ when $V_{in1} = V_{in2}$!!

What causes offset?



Random asymmetries during fabrication and packaging

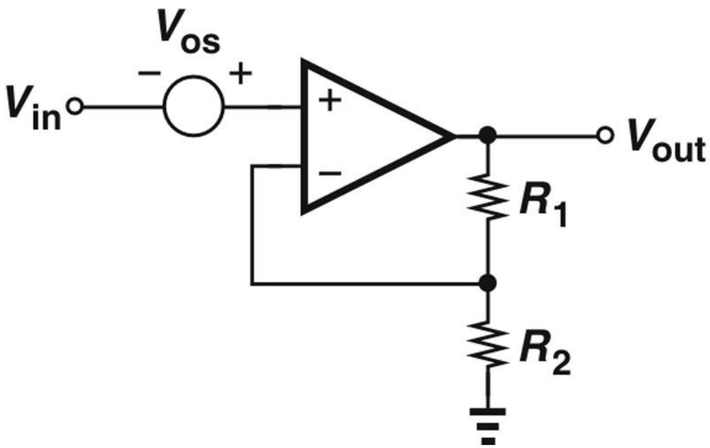


Model the offset by a single voltage source placed in series with one of the inputs

- Offsets in an op amp that arise from input stage mismatch cause the input-output characteristic to shift in either the positive or negative direction (the plot displays positive direction).

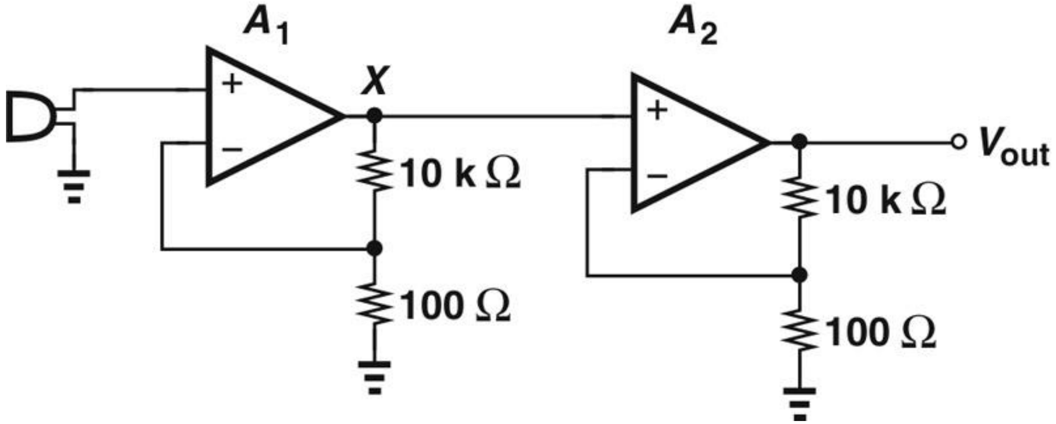
Effects of DC offsets

The offset is also amplified!!



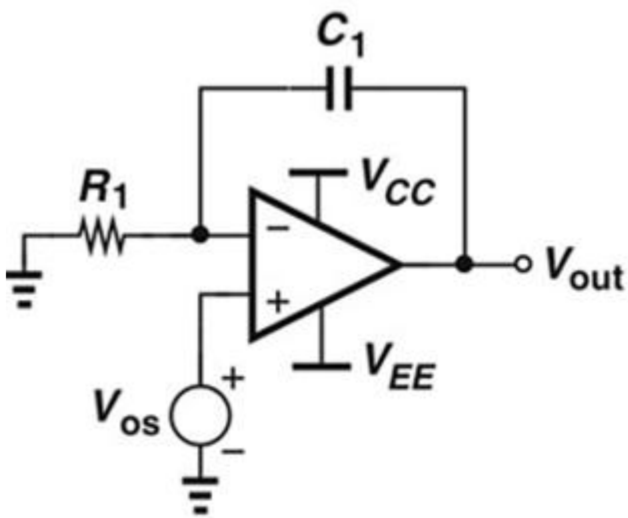
$$V_{out} = \left(1 + \frac{R_1}{R_2}\right)(V_{in} + V_{os})$$

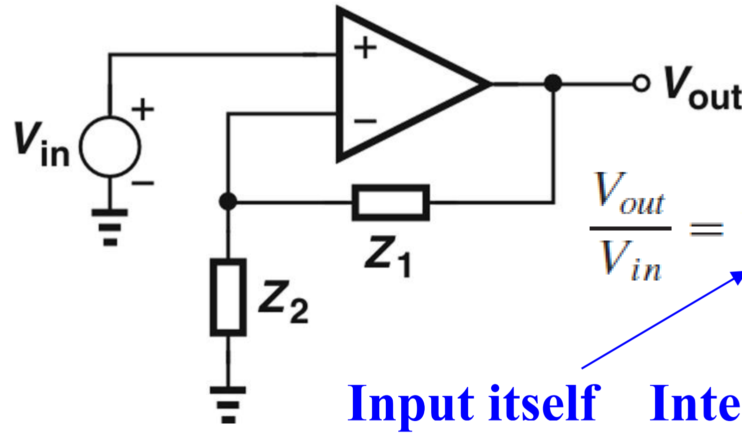
Saturation due to DC offsets



- 2mV offset at the input can cause saturation at the 2nd stage for 3V supply
- Offset amplification is cascaded stages can be resolved through ac coupling

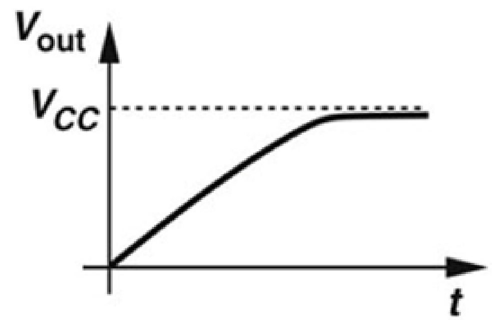
Offset in Integrator





$$\frac{V_{out}}{V_{in}} = 1 + \frac{Z_1}{Z_2}$$

Input itself **Integral of the input**

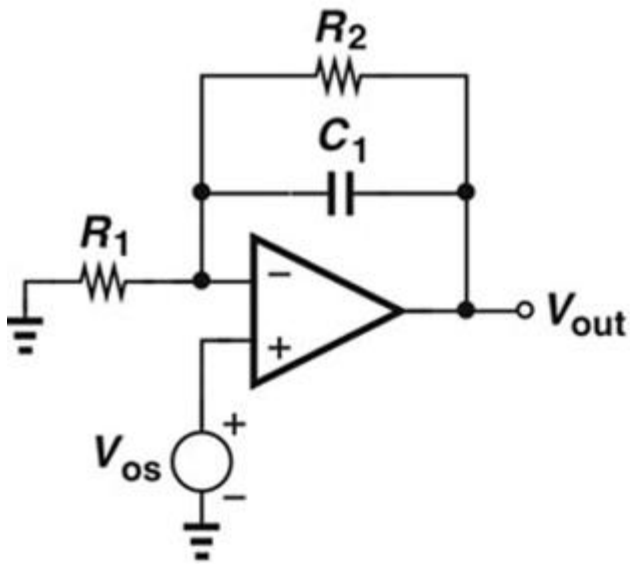


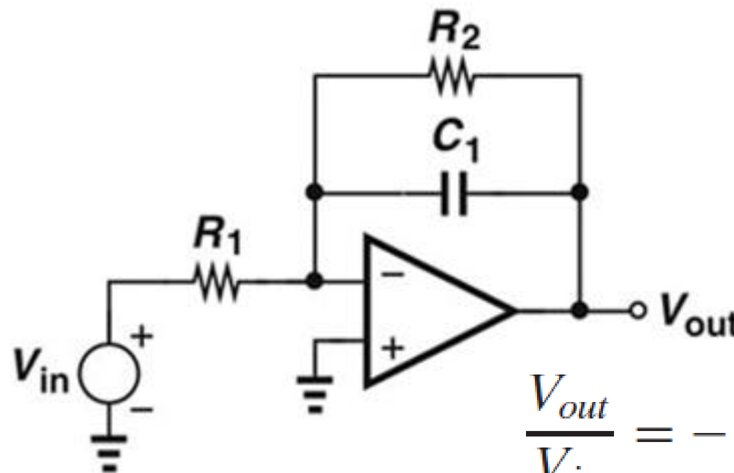
Noninverting configuration!!

$$V_{out} = V_{os} + \frac{1}{R_1C_1}\int_0^t V_{os}\,dt = V_{os} + \frac{V_{os}}{R_1C_1}t$$

- **The circuit generates an output that tends to +∞ or -∞ depending on the sign of V_{OS}.**
- **V_{out} would eventually approaches to power rails and saturates.**

To Reduce Effect of Offset





$$\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}\frac{1}{R_2C_1s+1}$$

At low frequencies

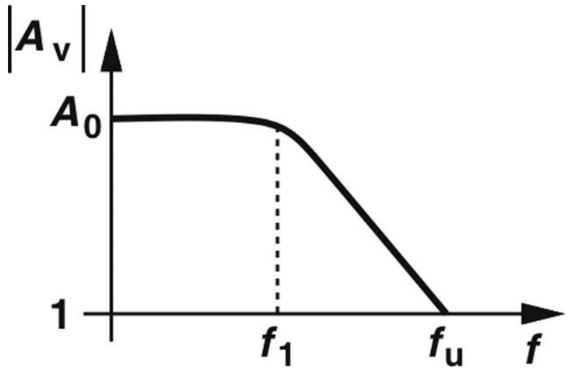
$$V_{out} = V_{os}\left(1+\frac{R_2}{R_1}\right)$$

For high frequency that $R_2C_1s >> 1$

$$\frac{V_{out}}{V_{in}} = -\frac{1}{R_1C_1s}$$

- **R2/R1 must be sufficiently small to minimize the amplified offset.**
- **R2C1 must be sufficiently large to negligibly impact the signal frequencies of interest.**

Finite Bandwidth



$$\frac{V_{out}}{V_{in1}-V_{in2}}(s)=\frac{A_0}{1+\frac{s}{\omega_1}}$$

- $s/\omega_1 \ll 1$, gain is A_0.
- $s/\omega_1 \gg 1$, gain falls to unity at $\omega_u = A_0\omega_1$.

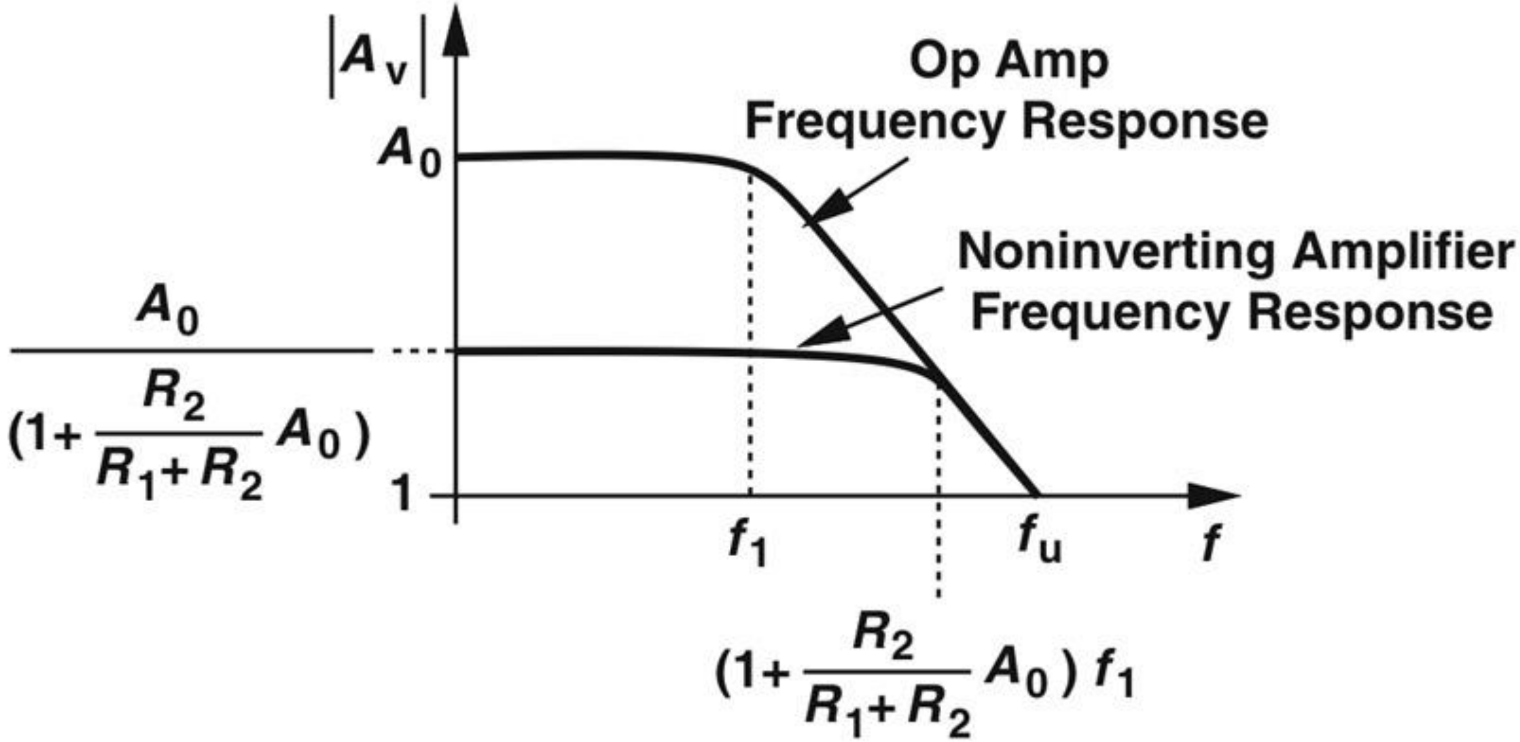
  ω_u : Unity-gain bandwidth of the op amp

<Reexamine the noninverting amplifier>

$$\frac{V_{out}}{V_{in}}=\frac{A_0}{1+\frac{R_2}{R_1+R_2}A_0} \Rightarrow \frac{V_{out}}{V_{in}}(s)=\frac{\frac{A_0}{1+\frac{s}{\omega_1}}}{1+\frac{R_2}{R_1+R_2}+\frac{A_0}{1+\frac{s}{\omega_1}}}$$

$$\Rightarrow \frac{V_{out}}{V_{in}}(s)=\frac{A_0}{\frac{s}{\omega_1}+\frac{R_2}{R_1+R_2}A_0+1} \qquad |\omega_{p,closed}|=\left(1+\frac{R_2}{R_1+R_2}A_0\right)\omega_1$$

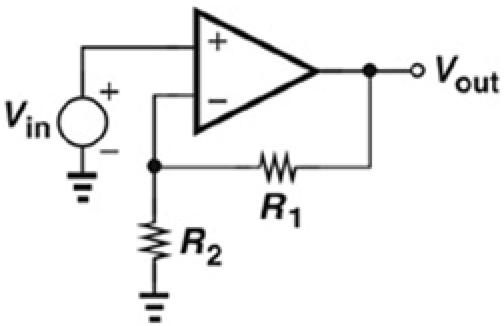
Bandwidth and Gain Tradeoff



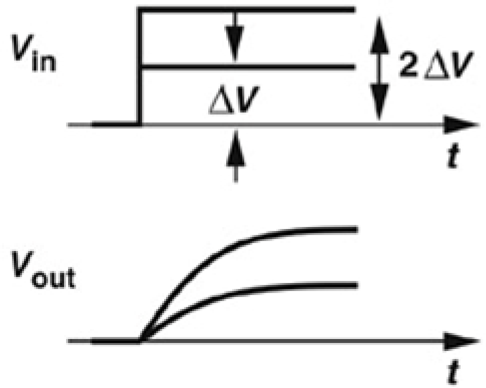
- **Having a loop around the op amp (inverting, noninverting, etc) helps to increase its bandwidth. However, it also decreases the low frequency gain.**

Slew Rate

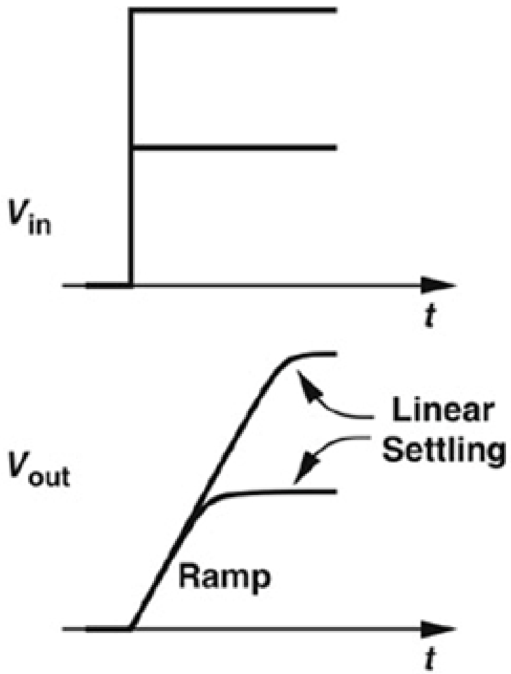
<Noninverting amplifier>



$$\frac{V_{out}}{V_{in}}(s) = \frac{A_0}{\frac{s}{\omega_1} + \frac{R_2}{R_1 + R_2}A_0 + 1}$$

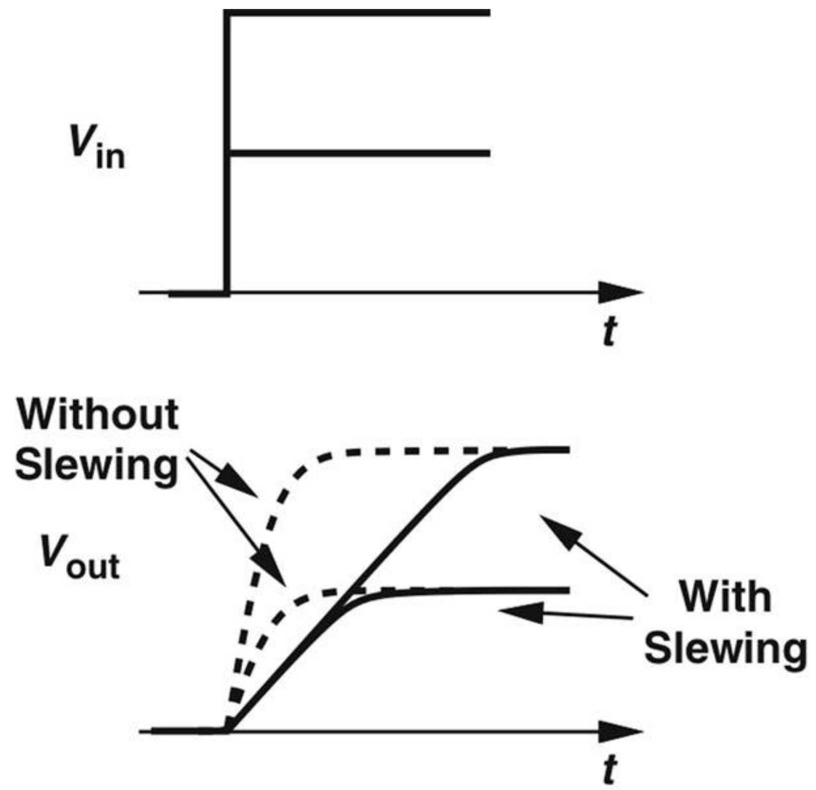


Time constant = $|\omega_{p,closed}|^{-1}$



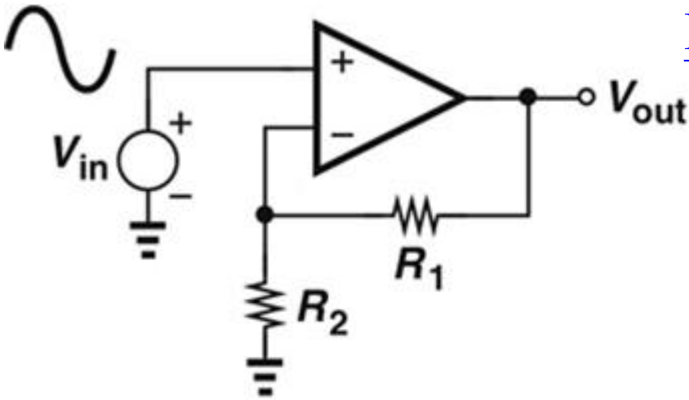
- **In the linear region, when the input doubles, the output and the output slope also double. However, when the input is large, the op amp slews so the output slope is fixed by a constant current source charging a capacitor.**
- **This further limits the speed of the op amp.**

Settling with and without Slew Rate

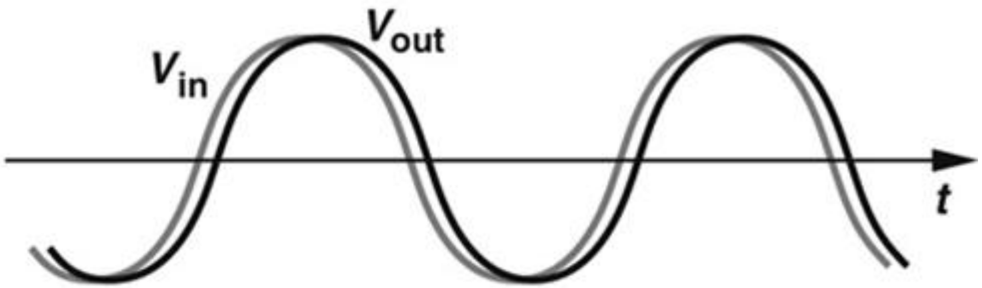


- **The settling speed is faster without slew rate (as determined by the closed-loop time constant).**
- **Slewing is a *nonlinear* phenomenon. (If x → y, then 2x ↛ 2y)**

Slew Rate Limit on Sinusoidal Signals



Low frequency signal, slew rate is sufficient



$$V_{in}(t) = V_0 \sin \omega t$$

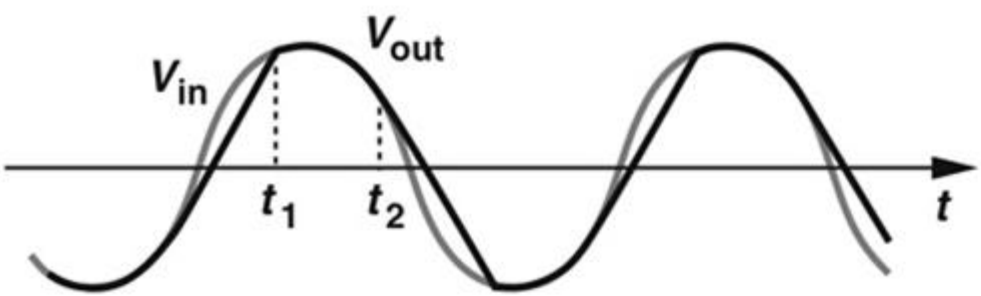
$$V_{out}(t) = V_0(1 + R_1/R_2) \sin \omega t$$

$$\Rightarrow \frac{dV_{out}}{dt} = \underline{V_0\left(1 + \frac{R_1}{R_2}\right)\omega} \cos \omega t$$

Maximum slope at zero crossing

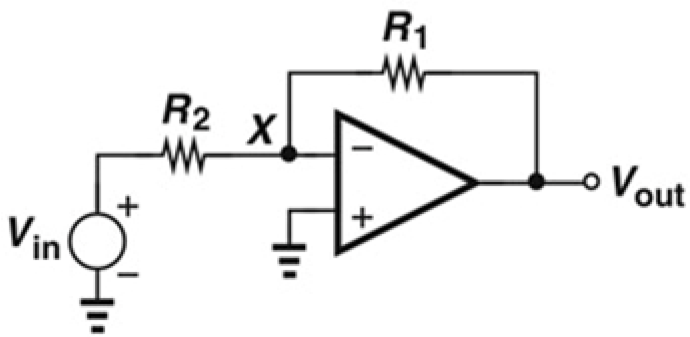
The op amp slew rate must exceed to avoid slewing.

Slew rate is insufficient



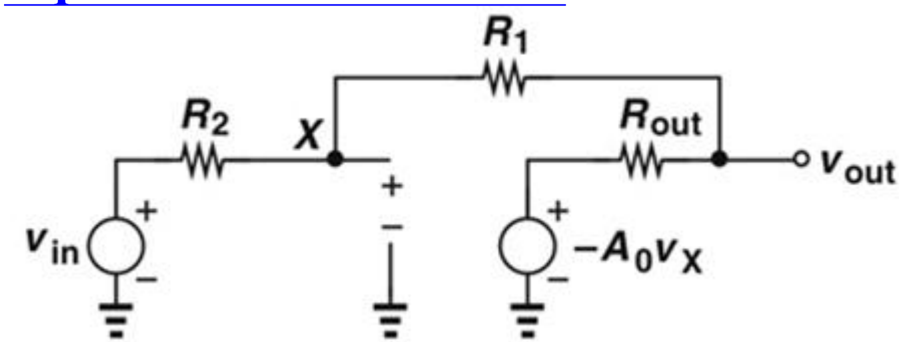
- **The output fails to follow while passing through zero.**
- **The output tracks between t_1 and t_2.**

Finite Input and Output Impedances



What happens if op amp has an output resistance R_{out}?

Equivalent circuit model



$$v_{in} + (R_1 + R_2)\frac{-A_0 v_X - v_{out}}{R_{out}} = v_{out}$$

$$v_X = \frac{R_2}{R_1 + R_2}(v_{out} - v_{in}) + v_{in}$$

$$\frac{V_{out}}{V_{in}} = -\frac{1}{\dfrac{R_2}{R_1} + \dfrac{1}{A_0}\left(1 + \dfrac{R_2}{R_1}\right)}$$

$$\Rightarrow \quad \frac{v_{out}}{v_{in}} = -\frac{R_1}{R_2}\,\frac{A_0 - \dfrac{R_{out}}{R_1}}{1 + \dfrac{R_{out}}{R_2} + A_0 + \dfrac{R_1}{R_2}}$$

Gain errors